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EXAMINER

VU, QUANG D

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 05/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/893,036

Applicant(s)

SATHE, AJIT V.

Examiner

Quang D Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on amendment filed on 04/28/03.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 17, 18, 21-23, 26, 27, 31-33, 36-40, 42, 44 and 46 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 17, 18, 21-23, 26, 27, 31-33, 36-40, 42, 44 and 46 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

The finality of the rejection of the last Office action is withdrawn in view of the present Office action.

#### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 23, 33, 36, 39, 42, 44 and 46 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23, in line 2, the phrase "...each comprising a plurality of traces" is unclear as to what structure comprising a plurality of traces. The phrase should change to "...each of the layers comprising a plurality of traces".

Claim 33, in line 2, the phrase "...each comprising a plurality of traces" is unclear as to what structure comprising a plurality of traces. The phrase should change to "...each of the layers comprising a plurality of traces".

Claim 36, in lines 1-2, the phrase "...the one or more vias couple traces within different layers" is unclear as to what layers is it being referred to. Is it being referred to the contiguous layers of claim 17.

Claim 39, in line 2, the phrase "...each comprising a plurality of traces" is unclear as to what structure comprising a plurality of traces. The phrase should change to "...each of the layers comprising a plurality of traces".

Claim 40, in lines 1-2, the phrase "...the one or more vias couple traces within different layers" is unclear as to what layers is it being referred to. Claim 37 never discloses any structure that has a plurality of different layers.

Claim 42, in lines 1-2, the phrase "...the one or more vias couple traces within different layers" is unclear as to what layers is it being referred to. Claim 21 never discloses any structure that has a plurality of different layers.

Claim 44, in lines 1-2, the phrase "...the one or more vias couple traces within different layers" is unclear as to what layers is it being referred to. Is it being referred to the contiguous layers of claim 26.

Claim 46, in lines 1-2, the phrase "...the one or more vias couple traces within different layers" is unclear as to what layers is it being referred to. Claim 31 never discloses any structure that has a plurality of different layers.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 17-18, 21-22, 26-27, 36-40, 42 and 44 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,407,929 to Hale et al.

Regarding claim 17, Hale et al. (figure 3) teach an electronic package substrate comprising:

a thin, flexible, electrically insulating film (a composite film [302] comprises flexible films [304, 310]) (column 4, lines 40 – 47) having a conductor region (306, 312, 316) to mount an integrated circuit (314);

a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]) within the film, including within the conductor region (306, 312, 316);

a plurality of lands (a portion of layer [316] which is in contact with the pad [322]) on a surface of the film and coupled to the traces (306, a portion of layer [316] which is not in contact with pad [322]), wherein the lands are to mount corresponding pads (322) of the integrated circuit (314) in a ball grid array (322); and

wherein the film (302) comprises a plurality of contiguous layers (layers [304, 306] are considered as one layer and the layer [310] and layer [316] are considered as another layer), selected ones of which comprises a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]), and wherein the film (302) comprises one or more vias (312) coupled to corresponding ones of the traces (306, a portion of layer [316] which is not in contact with pad [322]).

Regarding claim 18, Hale et al. teaches the film (302) is formed of material comprising an epoxy (column 4, lines 40-47).

Regarding claim 21, Hale et al. (figure 3) teaches an electronic package comprising:

a package substrate (302) including:

a thin, flexible, electrically insulating film (a composite film [302] comprises flexible films [304, 310]) (column 4, lines 40 – 47) having a conductor region (306, 312, 316) to mount an integrated circuit (314);

a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]), at least some of which are within the conductor region (306, 312, 316);

one or more vias (312) within the film and coupled to corresponding ones of the traces (306, a portion of layer [316] which is not in contact with pad [322]); and

a plurality of lands (a portion of layer [316] which is in contact with the pad [322]) on a surface of the film and coupled to the traces (306, a portion of layer [316] which is not in contact with pad [322]); and

an integrated circuit (314) having a plurality of pads (322) coupled to the plurality of lands (a portion of layer [316] which is in contact with the pad [322]) in a ball grid array (322).

Regarding claim 22, Hale et al. teaches the film (302) is formed of material comprising an epoxy (column 4, lines 40-47).

Regarding claim 26, Hale et al. (figure 3) teach an electronic system having at least one electronic assembly comprising:

a thin, flexible, electrically insulating film (a composite film [302] comprises flexible films [304, 310]) (column 4, lines 40 – 47) having a conductor region (306, 312, 316), a plurality of traces (306) in the conductor region, and a plurality of lands (316) coupled to the traces (306);

an integrated circuit (314) having a plurality of pads (322) coupled to the plurality of lands (316) in a ball grid array (322); and

wherein the film (302) comprises a plurality of contiguous layers (layers [304, 306] are considered as one layer and the layer [310] and layer [316] are considered as another layer), selected one of which comprise a plurality of traces (306) in the conductor region (306, 312, 316), and wherein the film (302) comprises one or more vias (312) coupled to corresponding ones of the traces (306).

Regarding claim 27, Hale et al. teaches the film (302) is formed of material comprising an epoxy (column 4, lines 40-47).

Regarding claim 36, Hale et al. teach the one or more vias (312) coupled traces (306, a portion of layer [316] which is not in contact with pad [322]) within different layers (304, 310).

Regarding claim 37, Hale et al. (figure 3) teach a package substrate comprising:

a thin, flexible, electrically insulating film (a composite film [302] comprises flexible films [304, 310]) (column 4, lines 40 – 47) having a conductor region (306, 312, 316) to mount an integrated circuit (314);

a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]), at least some of which are within the conductor region (306, 312, 316);

one or more vias (312) within the film (302) and coupled to corresponding ones of the traces (306, a portion of layer [316] which is not in contact with pad [322]); and

a plurality of lands (a portion of layer [316] which is in contact with the pad [322]) on a surface of the film (302) and coupled to the traces (306, a portion of layer [316] which is not in

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contact with pad [322]), wherein the lands are to mount corresponding pads (322) of the integrated circuit (314).

Regarding claim 38, Hale et al. teaches the film (302) is formed of material comprising an epoxy (column 4, lines 40-47).

Regarding claim 39, Hale et al. teach the film (302) comprises a plurality of layers (layers [304, 306] are considered as one layer and the layer [310] and layer [316] are considered as another layer), each of the layers comprising a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]) in the conductor region (306, 312, 316).

Regarding claim 40, Hale et al. teach the one or more vias (312) coupled traces (306, a portion of layer [316] which is not in contact with pad [322]) within different layers (304, 310).

Regarding claim 42, Hale et al. teach the one or more vias (312) coupled traces (306, a portion of layer [316] which is not in contact with pad [322]) within different layers (304, 310).

Regarding claim 44, Hale et al. teach the one or more vias (312) coupled traces (306, a portion of layer [316] which is not in contact with pad [322]) within different layers (304, 310).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.



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6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,407,929 to Hale et al.

Regarding claim 23, Hale et al. teach the film (302) comprises a plurality of layers (layers [304, 306] are considered as one layer and the layer [310] and layer [316] are considered as another layer), each comprising a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]) in the conductor region (306, 312, 316). Hale et al. differ from the claimed invention by not showing each layer has a thickness within the range of approximately 0.15 to 0.30 millimeters. It would have been obvious to one having ordinary skill in the art at the time the invention was made for each layer has a thickness within the range of approximately 0.15 to 0.30 millimeters, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. Claims 31-33 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,365,421 to Debenham et al. in view of US Patent No. 6,407,929 to Hale et al.

Regarding claim 31, Debenham et al. (figure 1) teach microprocessor (12), bus (18), display (24) and memory (14). Debenham et al. differ from the claimed invention by not showing a processor comprising an electronic assembly including, a thin, flexible electrically insulating film having a conductor region, a plurality of traces in the conductor region, one or more vias coupled to corresponding ones of the traces, and a plurality of lands coupled to the traces; and an integrated circuit having a plurality of pads coupled to the plurality of lands. However, Hale et al. teach a thin, flexible electrically insulating film (a composite film [302]

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comprises flexible films [304, 310]) (column 4, lines 40 – 47) having a conductor region (306, 312, 316), a plurality of traces (306, 316) in the conductor region (306, 312, 316), one or more vias (312) coupled to corresponding ones of the traces (306, a portion of layer [316] which is not in contact with pad [322]), and a plurality of lands (a portion of layer [316] which is in contact with the pad [322]) coupled to the traces (306, a portion of layer [316] which is not in contact with pad [322]); and an integrated circuit (314) having a plurality of pads (322) coupled to the plurality of lands (316). It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Hale et al. into the device taught by Debenham et al., since it is desirable to add functionality to the device.

Regarding claim 32, the combined device shows the film is formed of material comprising an epoxy.

Regarding claim 33, the combined device shows the film (302) comprises a plurality of layers (layers [304, 306] are considered as one layer and the layer [310] and layer [316] are considered as another layer), each of the layers comprising a plurality of traces (306, a portion of layer [316] which is not in contact with pad [322]) in the conductor region (306, 312, 316).

Regarding claim 46, the combined device shows one or more vias (312) coupled traces (306, a portion of layer [316] which is not in contact with pad [322]) within different layers (304, 310).

### ***Conclusion***

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv  
May 23, 2003

Steven Loto  
Primary Examiner  
*Steven Loto*